In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 27 (Cancelled)

28. (Currently Amended) ~~The~~ A data processing apparatus ~~of claim 25, further~~ comprising:

a first multiply circuit having first and second inputs and an output, said first multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a first product at said output;

a first Q shifter having an input receiving said first product from said first multiply circuit and an output ~~supplying said first input to said adder/subtractor circuit~~, said first Q shifter shifting said first product an instruction specified number of bits responsive to the rounding dot product instruction; ~~and~~

a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output;

a second Q shifter having an input receiving said second product from said second multiply circuit and an output ~~supplying said second input to said adder/subtractor circuit~~, said second Q shifter shifting said second product said instruction specified number of bits responsive to the rounding dot product instruction;

an adder/subtractor circuit having first and second inputs, a mid-position carry input to a predetermined bit and an output, said first input receiving said shifted first product from first Q shifter, said second input receiving said shifted second product from said second Q shifter, said adder/subtractor circuit operable in response to said dot product instruction to arithmetically

combine said first and second products and a "1" input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum; and

a shifter connected to receive said mid-position rounded sum of the adder/subtractor circuit, the shifter operable to shift said mid-position rounded sum a predetermined amount in response to said dot product instruction.

29. (Currently Amended) ~~The~~ A data processing apparatus ~~of claim 25, wherein~~ comprising:

a first multiply circuit having first and second inputs and an output, said first multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a first product at said output, said first multiply ~~generates~~ generating said first product in a redundant sign/magnitude format;

a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output, said second multiply circuit ~~generates~~ generating said second product in said redundant sign/magnitude format;

an adder/subtractor circuit having first and second inputs, a mid-position carry input to a predetermined bit and an output, said first input receiving said first product from said first multiply circuit, said second input receiving said second product from said second multiply circuits, said adder/subtractor circuit operable in response to said dot product instruction to arithmetically combine said first and second products and a "1" input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum, said adder/subtractor circuit arithmetically ~~combines~~ combining said first and second products

and said "1" input at said mid-position carry input forming said mid-position rounded sum in said redundant sign/magnitude format;

a shifter connected to receive said mid-position rounded sum of the adder/subtractor circuit, the shifter operable to shift said mid-position rounded sum a predetermined amount in response to said dot product instruction, said shifter ~~shifts~~ shifting said mid-position rounded sum in said redundant sign/magnitude format; and

~~said data processing apparatus further comprises~~ a carry save adder to 2's complement converter having an input receiving said shifted mid-position rounded sum in said redundant sign/magnitude format from said shifter and an output generating a corresponding normal coded format.